

What is Claimed is:

1. An interface unit controlling the exchange of signals between a data processing unit and a communication bus, the interface unit comprising:

5 a receive channel for receiving data groups from the communication bus and the applying the data groups to the data processing unit; and

a transmit channel for receiving data groups from the data processing unit and applying the signal groups to a communication bus, wherein the interface unit can function in an ATM interface mode and can function in an I/O interface mode.

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2. The interface unit as recited in claim 1 wherein the interface unit can function in a UTOPIA ATM interface mode and can function in an I/O interface mode.

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3. The interface unit as recited in claim 1 wherein the interface unit exchanges data groups with the direct memory access unit of the data processing unit.

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4. The interface unit as recited in claim 1 further comprising a control register, the control register determining when the interface unit is in the ATM mode of operations and when the interface unit is in the I/O mode of operation.

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5. The interface unit as recited in claim 1 wherein the interface unit includes: an input interface unit;

an output interface unit;

an input buffer memory unit, wherein the transfer between the input buffer

memory unit and the direct memory access unit is determined by a receive event signal; and

an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal.

6. The interface unit as recited in claim 1 wherein the UTOPIA ATM URDATA signal corresponds to an I/O OUTDATAVALID signal, and wherein a UTOPIA ATM UXCLAV signal corresponds to an I/O INDATAVALID signal.

5 7. A method of exchanging data groups between a communication bus and a data processing system, the method comprising:

in response to a first set of signals in an interface unit, exchanging data groups in a ATM mode of operation; and

10 in response to a second set of signals in the interface unit, exchanging data groups in an I/O mode of operation.

8. The method as recited in claim 7 wherein exchanging data groups includes exchanging data groups in a UTOPIA AMT mode of operation.

15 9. The method as recited in claim 8 wherein the processor is a digital signal processor.

10. The method as recited in claim 8 further comprising implementing the interface unit including:

20 an input interface unit;

an output interface unit;

an input buffer memory unit, wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal; and

25 an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal.

30 11. The method as recited in claim 10 further including storing the first and the second set of signals in a control register in the interface unit.

12. The method as recited in claim 11 wherein the UTOPIA ATM URDATA signal corresponds to an I/O OUTDATAVALID signal, and wherein a UTOPIA ATM UXCLAV signal corresponds to an I/O INDATAVALID signal.

5        13. A data processing unit comprising:  
a connector for coupling to a communication bus;  
a processor; and  
an interface unit implementing the exchange of data groups between the connector and the processor; the interface unit including a control register, the interface 10 unit operating in an ATM mode when a first set of signals are stored in the control register, the interface unit operating in an I/O mode when a second set of signals are stored in the control register.

15        14. The data processing system as recited in claim 13 wherein the interface unit operates in a UTOPIA ATM mode when the first set of signals are stored in the control register.

20        15. The interface unit as recited in claim 13, the interface unit including:  
an input interface unit;  
an output interface unit;  
an input buffer memory unit; wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal;  
and  
an output buffer memory unit, wherein the transfer between the direct memory 25 access unit and the output buffer memory unit is determined by a transmit event signal.

30        16. The data processing unit as recited in claim 13 wherein the processor includes a direct memory access unit, the interface unit coupled between the direct memory access unit and the connector.

17. The data processing unit as recited in claim 13 wherein the UTOPIA ATM URDATA signal corresponds to an I/O OUTDATAVALID signal, and wherein a UTOPIA ATM UXCLAV signal corresponds to an I/O INDATAVALID signal.